AMENDMENTS TO THE CLAIMS

Please accept amended Claim 1 as follows:

1. (Currently Amended) A gated diode memory cell comprising:

at least one transistor having a diffusion region and a gate terminal connected directly to a write wordline; and

a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline.

2. (Previously Presented) A gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode forms one terminal of a storage cell and the second terminal of the gated diode forms another terminal of the storage cell.

3. (Previously Presented) A gated diode memory cell as defined in Claim 2 wherein the first terminal is a gate of the gated diode, wherein the gate is implemented in the form of a shallow trench.

4. (Previously Presented) A gated diode memory cell as defined in Claim 3, wherein the gate of the gated diode comprises a poly trench surrounded by thin oxide with silicon disposed underneath and surrounding the thin oxide.

5. (Original) A gated diode memory cell as defined in Claim 4 wherein the poly trench is cylindrical.

6. (Previously Presented) A gated diode memory cell as defined in Claim 4, wherein the gate of the gated diode comprises a metal oxide semiconductor ("MOS") capacitor.

7. (Original) A gated diode memory cell as defined in Claim 2 wherein the gate of the gated diode is planar.

8. (Original) A gated diode memory cell as defined in Claim 7 wherein the gate of the gated diode is disposed above a diffusion area.

9. (Original) A gated diode memory cell as defined in Claim 8, further comprising an oxide layer disposed between the gate of the gated diode and the diffusion area.

10. (Previously Presented)A gated diode memory cell as defined in Claim 7, wherein the gated diode comprises a planar metal oxide semiconductor ("MOS") capacitor.

11. (Withdrawn, Previously Presented) A gated diode memory cell as defined in Claim 1 wherein:

the at least one transistor is a field effect transistor ("FET"); and

the first terminal of the gated diode is a gate in signal communication with the source of the FET.

12. (Withdrawn) A gated diode memory cell as defined in Claim 11, further comprising a metal connector in signal communication between the source of the field effect transistor and the gate of the gated diode.

13. (Withdrawn) A gated diode memory cell as defined in Claim 12 wherein the metal connector is a direct metal connector ("MCBAR").

14. (Withdrawn, Previously Presented) A gated diode memory cell as defined in Claim 11 wherein:

the gate of the gated diode forms one terminal of a storage cell; and

the second terminal of the gated diode is a source of the gated diode that forms another terminal of the storage cell.

15. (Withdrawn) A gated diode memory cell as defined in Claim 14 wherein:

the drain of the FET is in signal communication with a bitline ("BL"); and

the gate of the FET is in signal communication with a write wordline ("WLw").

16. (Withdrawn, Previously Presented) A gated diode memory cell as defined in Claim 15 wherein the source of the gated diode is in signal communication with a read wordline ("WLr").

17. (Withdrawn, Previously Presented) A gated diode memory cell as defined in Claim 1 wherein:

the at least one transistor comprises first and second FETs with the source terminal of the first in signal communication with the gate terminal of the second; and

the first terminal of the gated diode is a gate of the gated diode in signal communication with the source terminal of the first FET.

18. (Withdrawn) A gated diode memory cell as defined in Claim 17 wherein:

the at least one transistor is a field effect transistor ("FET"); and

the gate of the gated diode is in signal communication with the source of the FET.

19. (Withdrawn) A gated diode memory cell as defined in Claim 18 wherein:

the gate of the gated diode forms one terminal of the storage cell; and

at least one of the source of the gated diode forms another terminal of the storage cell.

20. (Withdrawn) A gated diode memory cell as defined in Claim 19 wherein:

the drain of the FET is in signal communication with a bitline ("BL"); and

the gate of the FET is in signal communication with a write wordline ("WLw").

21. (Withdrawn) A gated diode memory cell as defined in Claim 20 wherein the bitline is a combined bitline in signal communication with a drain of an another FET in a single read/write configuration.

22. (Withdrawn) A gated diode memory cell as defined in Claim 20 wherein the bitline is a separated bitline in a dual read/write configuration.

23. (Withdrawn) A gated diode memory cell as defined in Claim 17 wherein:

The gate of the gated diode forms one terminal of the storage cell and at least one of the source of the gated diode forms another terminal of the storage cell.

24. (Withdrawn) A gated diode memory cell as defined in Claim 23 wherein:

the drain of the first FET is in signal communication with a bitline ("BL"); and

the gate of the first FET is in signal communication with a write wordline ("WLw").

25. (Withdrawn) A gated diode memory cell as defined in Claim 23 wherein at least one of the source of the gated diode is in signal communication with a read wordline ("WLr").

26. (Withdrawn, Previously Presented) A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises an implementing FET.

27. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is left open.

28. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the source of the implementing FET for the gated diode is left open, and the drain of the implementing FET for the gated diode becomes the source of the gated diode.

29. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is connected to the source of the implementing FET for gated diode.

30. (Withdrawn) A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises at least one "partial" FET.

31. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is left open to form one "partial" FET with the gate and source.

32. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the source of the gated diode FET is left open to form one "partial" FET with the gate and drain, and the drain of the gate diode FET becomes the source of the gated diode.

33. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is connected to the source of the gated diode FET to form two "partial" FETs in parallel.

34.~53 (Canceled)

54. (Withdrawn, Previously Presented) A gate diode memory cell as defined in claim 1, wherein the gated diode is a two terminal active device which has a first capacitance when a voltage on the first terminal relative to the second terminal is in a first voltage range, and which has a second capacitance when the voltage on the first terminal relative to the second terminal is in a second voltage range, wherein said first and second voltage ranges are defined by a threshold voltage of the gated diode.

55. (Withdrawn, Previously Presented) A gate diode memory cell as defined in claim 1, wherein the gated diode is a two terminal active device which has a first capacitance when a voltage on the first terminal relative to the second terminal is above a threshold voltage of the gated diode, and which has a second capacitance, which is less than the first capacitance, when the voltage on the first terminal relative to the second terminal is below the threshold voltage.

56.~ 57 (Canceled)

58. (Previously Presented) A gated diode memory cell as defined in Claim 1 wherein the at least one transistor and gated diode are a same type of FET (field effect transistor).